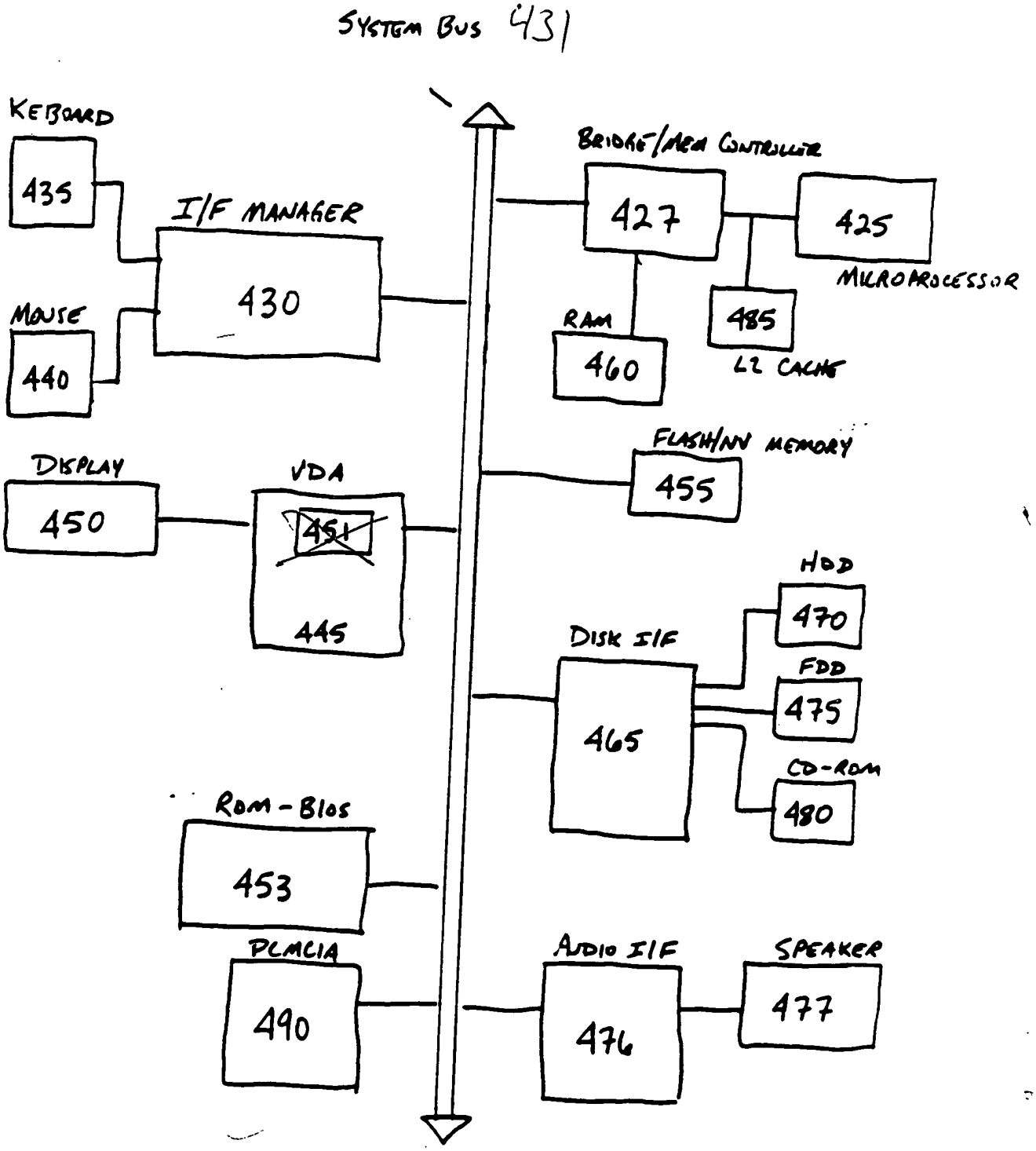


FIG 1

TD-152

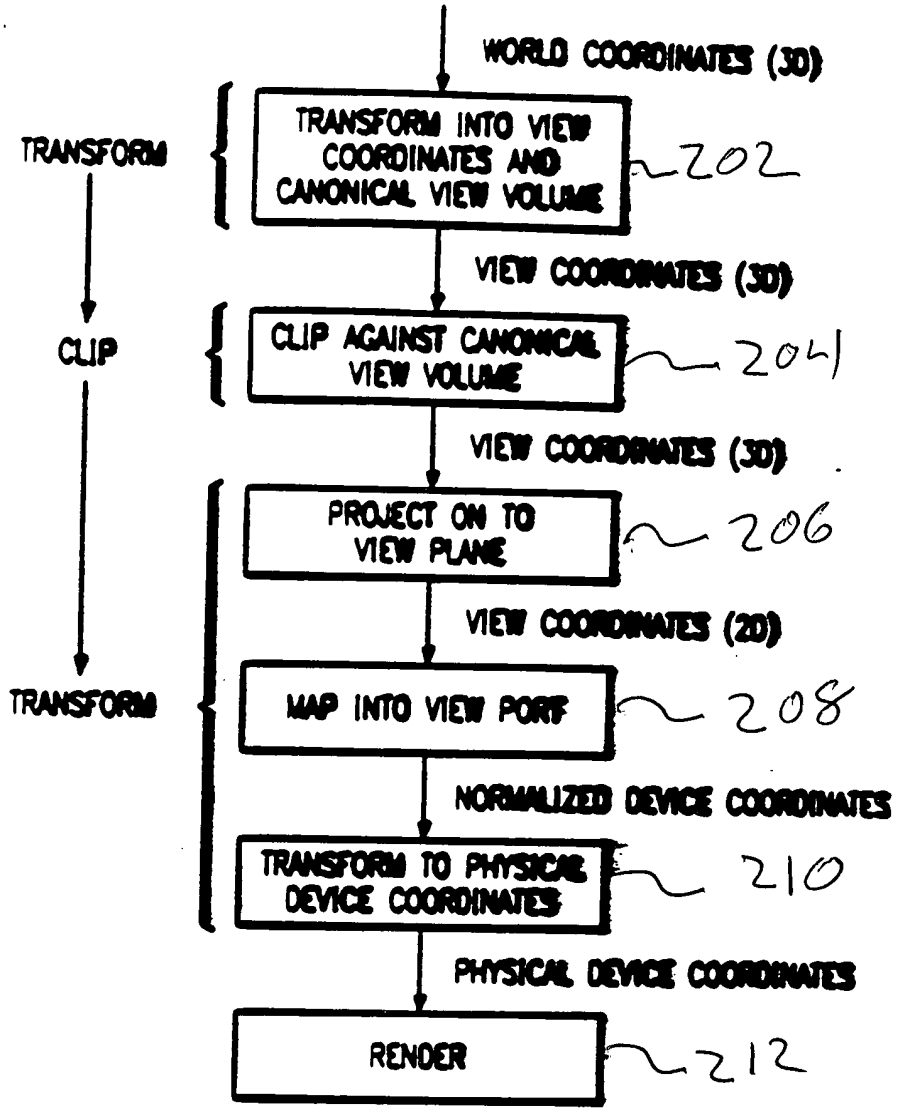


FIG. 2

TD-152

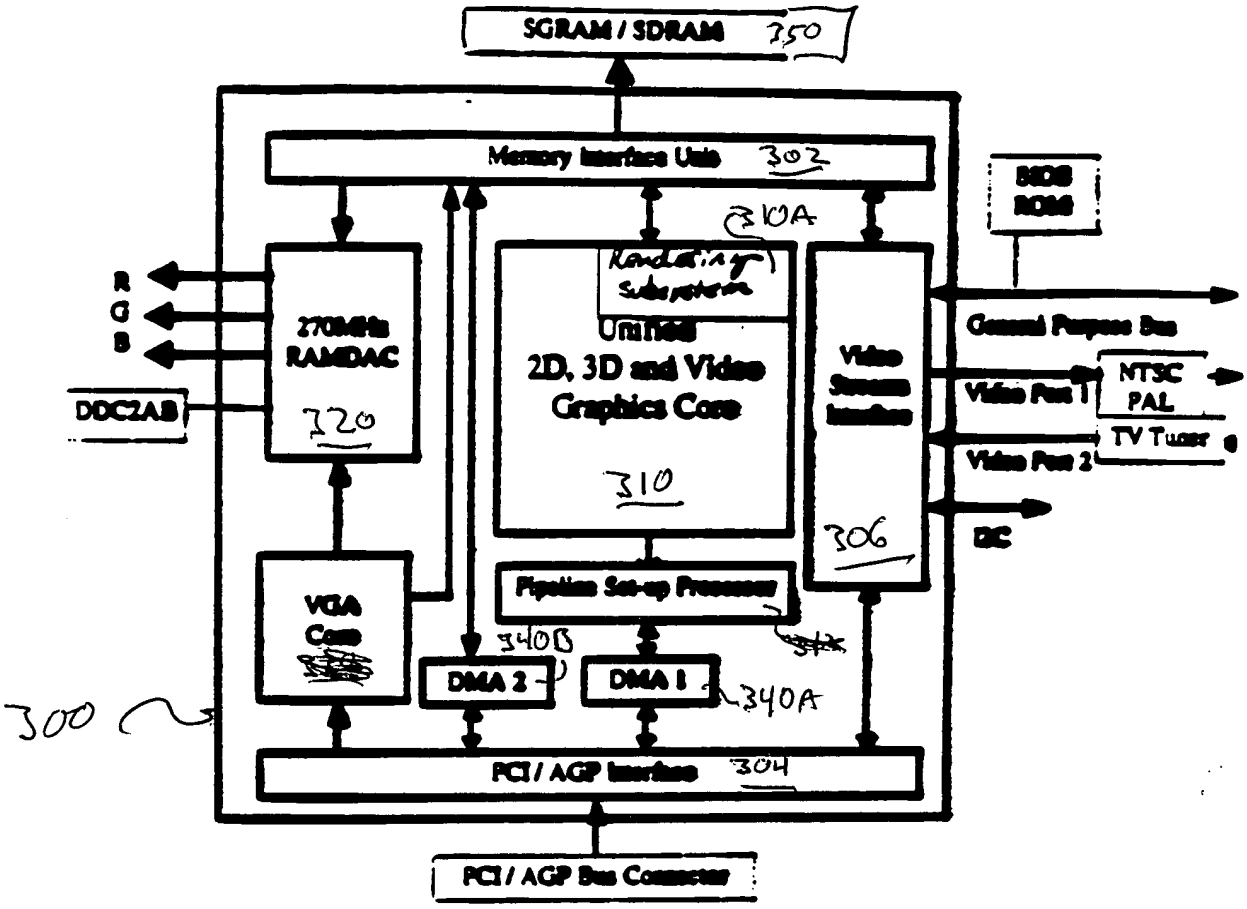


Figure 3

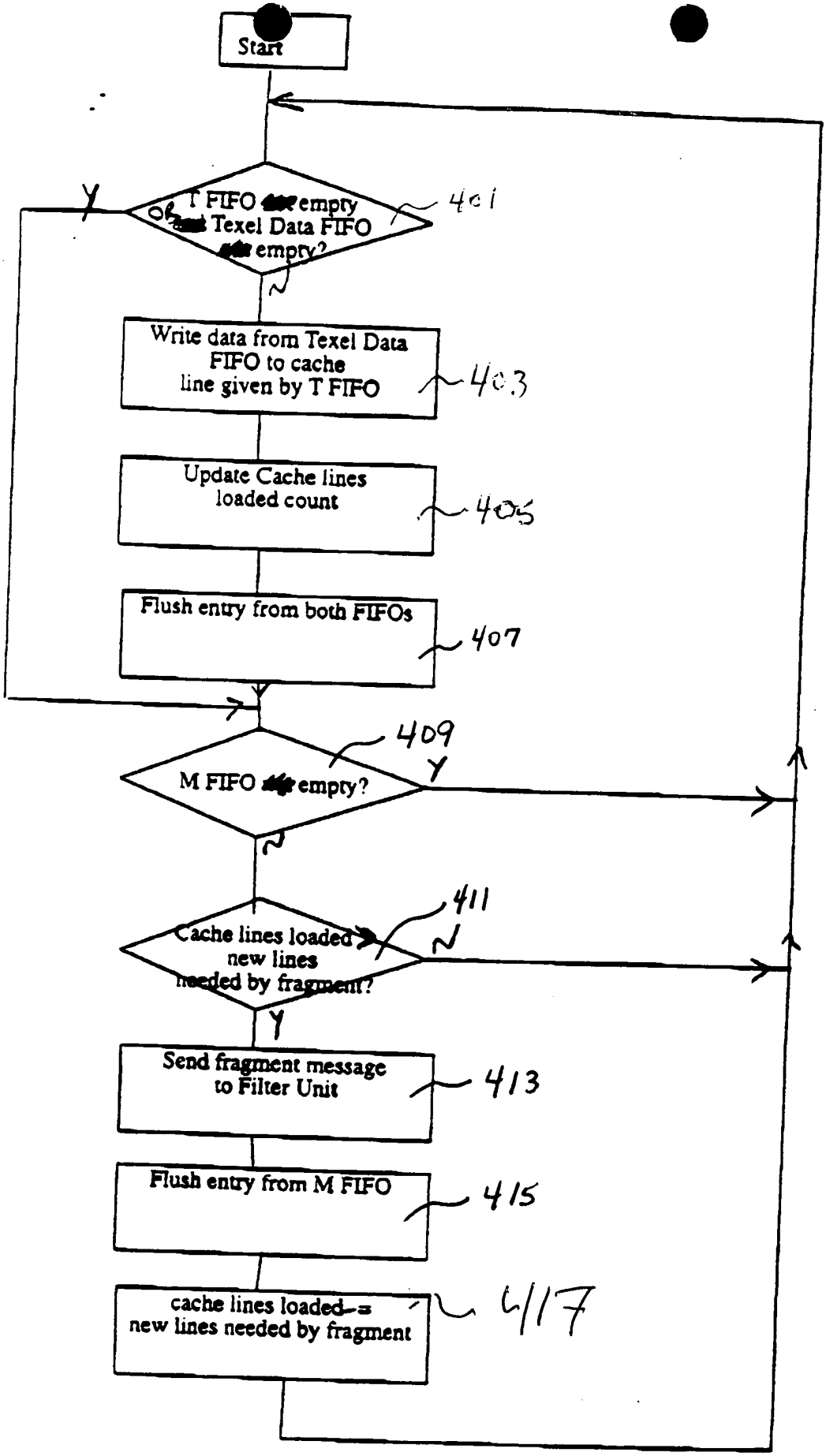


FIG. 4A

TD-152

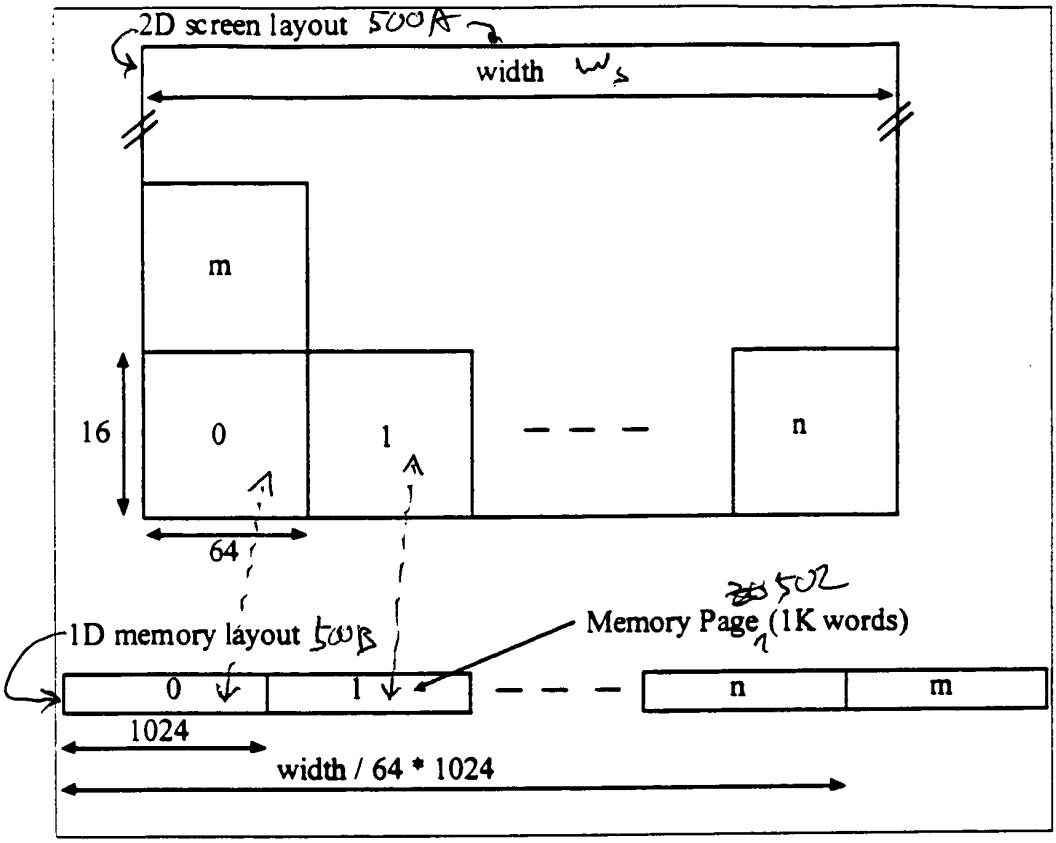


FIG. 5

Texture Map 600

Filter register assignment 602

Texel Coordinates 604

T0 (0,4)	T1 (1,4)	T0 (2,4)	T1 (3,4)	T0 (4,4)	T1 (5,4)	T0 (6,4)	T1 (7,4)	T0 (8,4)	T1 (9,4)
T2 (0,3)	T3 (1,3)	T2 (2,3)	T3 (3,3)	T2 (4,3)	T3 (5,3)	T2 (6,3)	T3 (7,3)	T2 (8,3)	T3 (9,3)
T0 (0,2)	T1 (1,2)	T0 (2,2)	T1 (3,2)	T0 (4,2)	T1 (5,2)	T0 (6,2)	T1 (7,2)	T0 (8,2)	T1 (9,2)
T2 (0,1)	T3 (1,1)	T2 (2,1)	T3 (3,1)	T2 (4,1)	T3 (5,1)	T2 (6,1)	T3 (7,1)	T2 (8,1)	T3 (9,1)
T0 (0,0)	T1 (1,0)	T0 (2,0)	T1 (3,0)	T0 (4,0)	T1 (5,0)	T0 (6,0)	T1 (7,0)	T0 (8,0)	T1 (9,0)

610

612

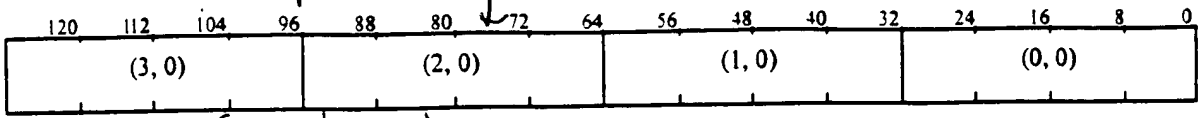
614

- 32 bit texels in memory word (610)
- 16 bit texels in memory word (612)
- 8 bit texels in memory word (614)

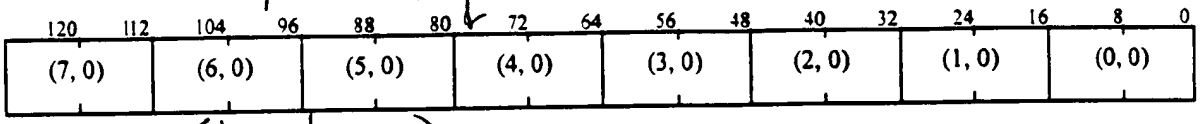
FIG. 6

Linear or Patch64 Memory Layouts

32 bits per texel (Layout 702)



16 bits per texel (Layout 704)



8 bits per texel (Layout 706)

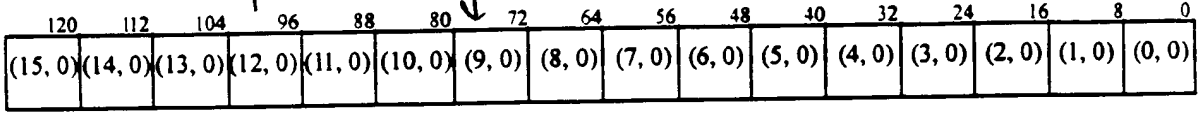
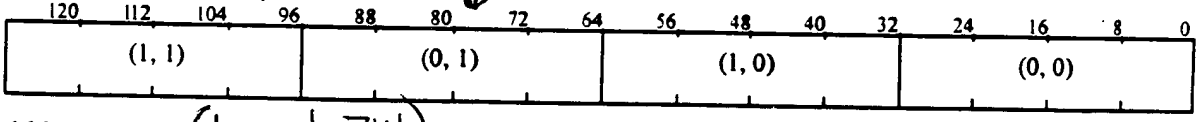


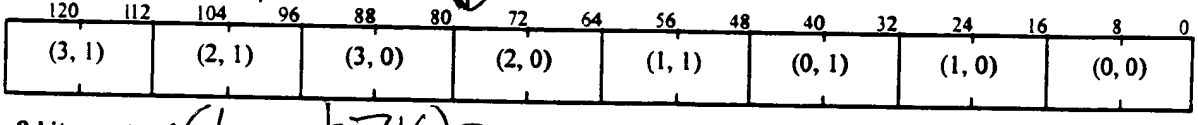
FIG. 7A

Patch32_2 or Patch2 Memory Layouts

32 bits per texel (Layout 712)



16 bits per texel (Layout 714)



8 bits per texel (Layout 716)

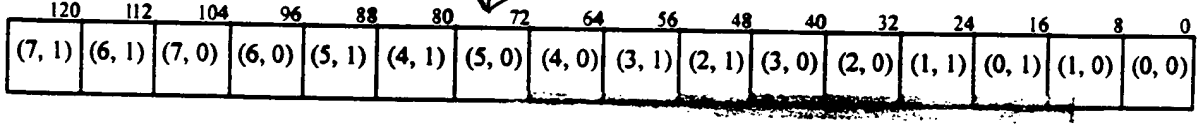


FIG. 7B

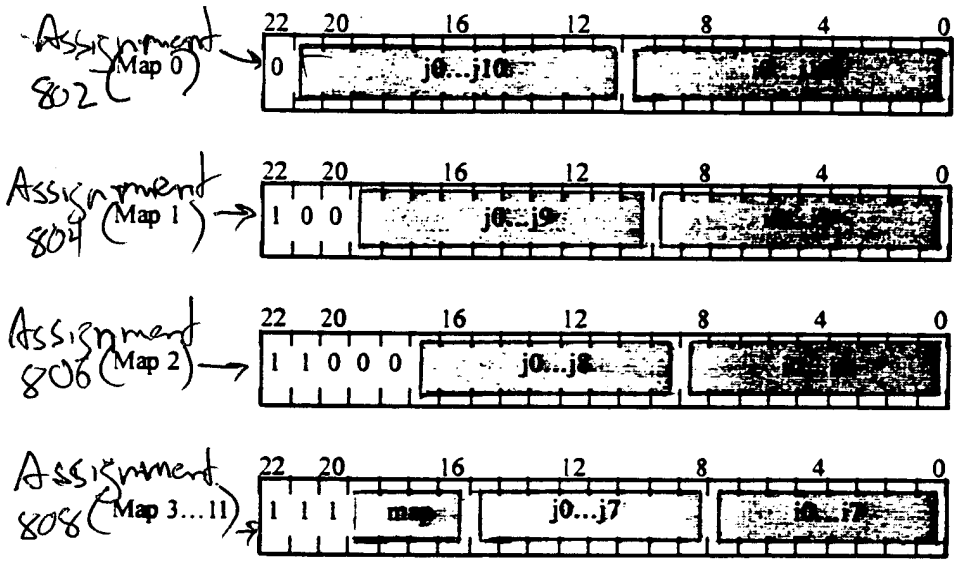


FIG. 8

TD-152

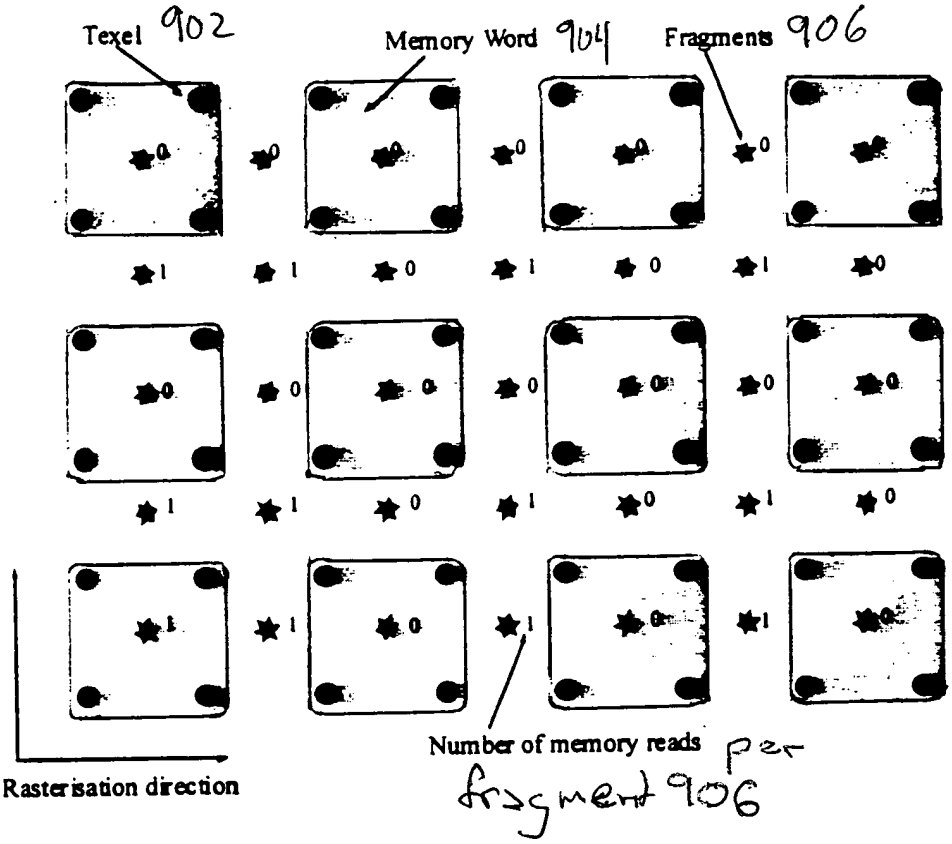


FIG. 9

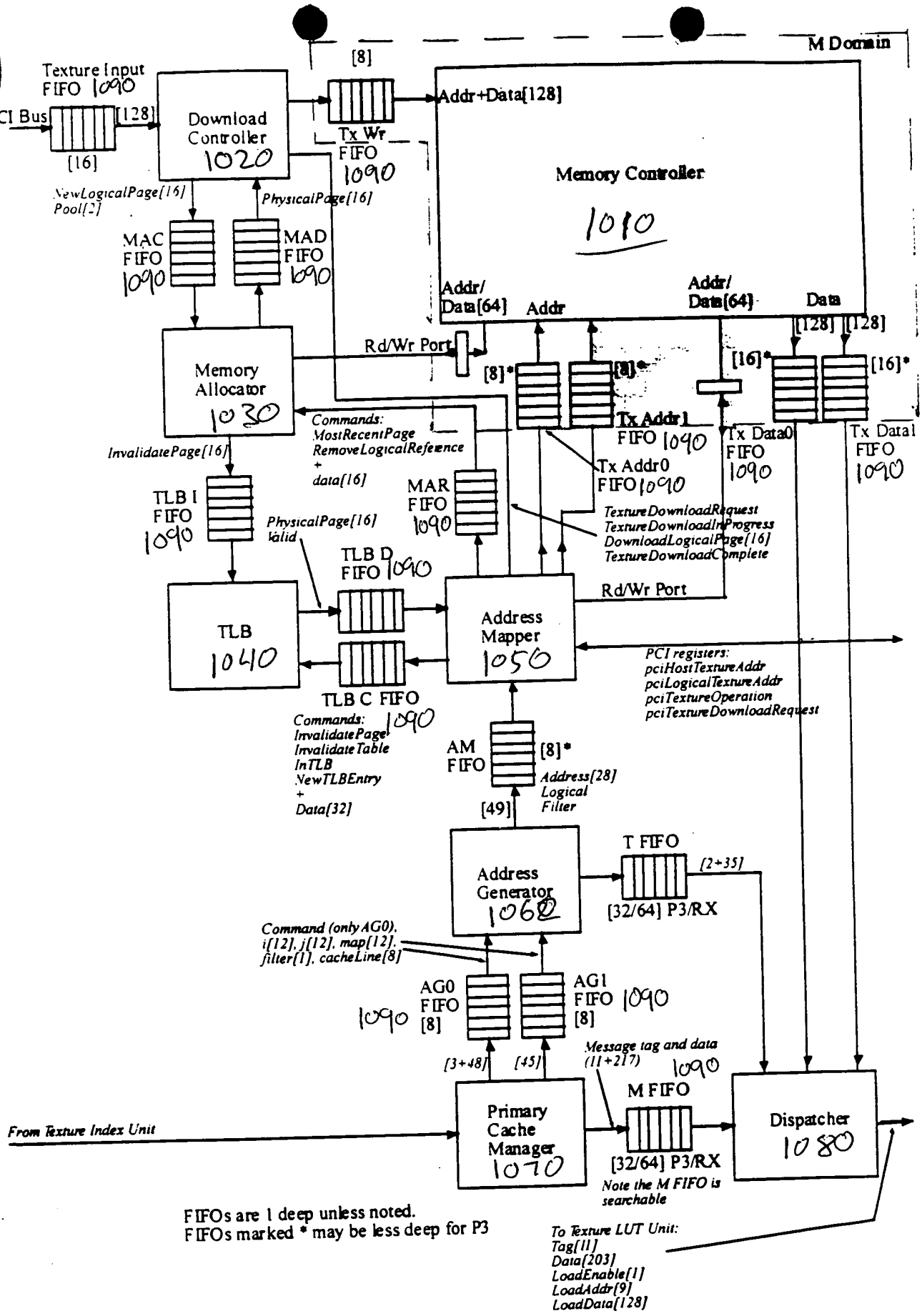


FIG. 10

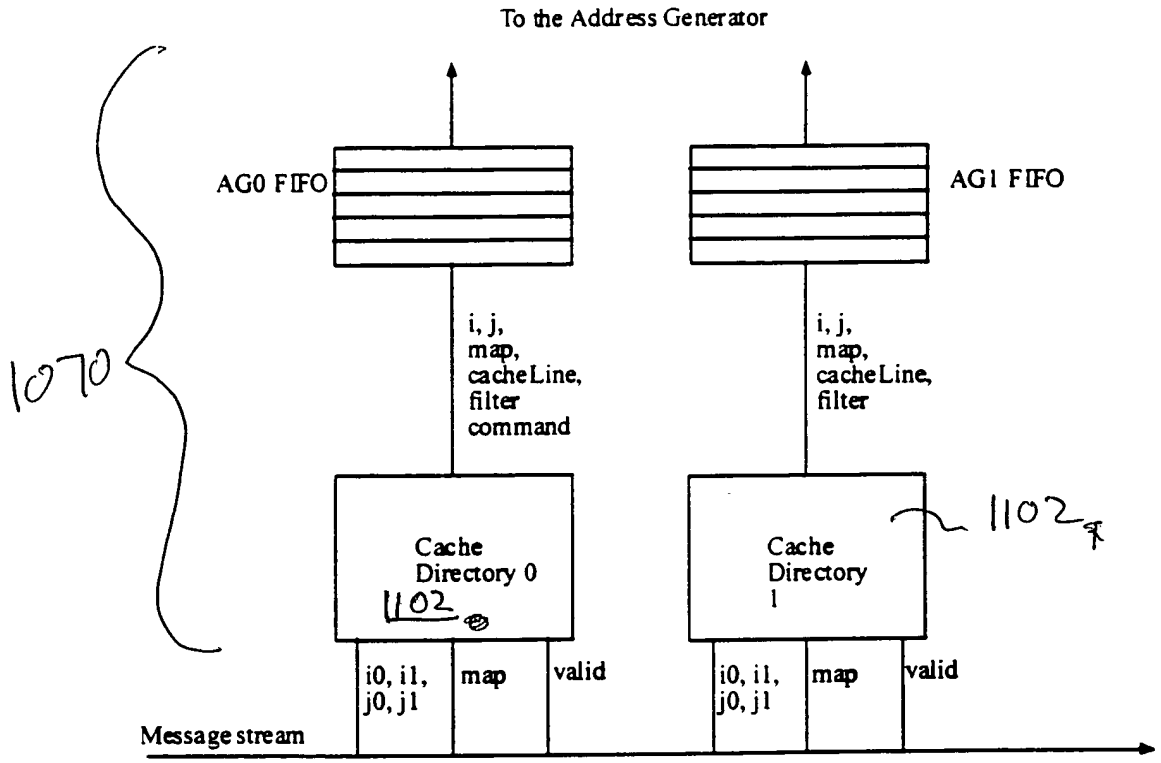


FIG. 11

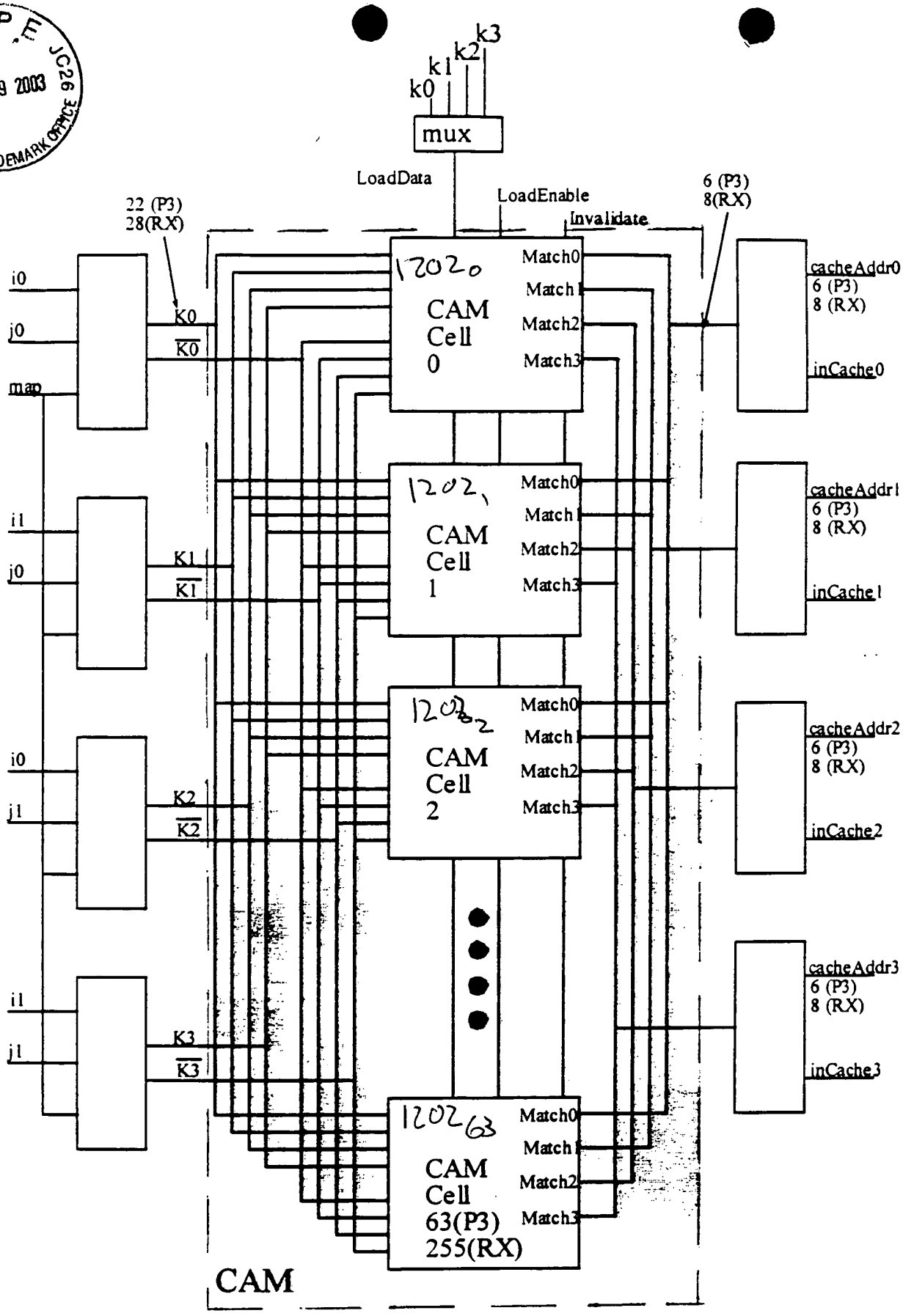


FIG 12

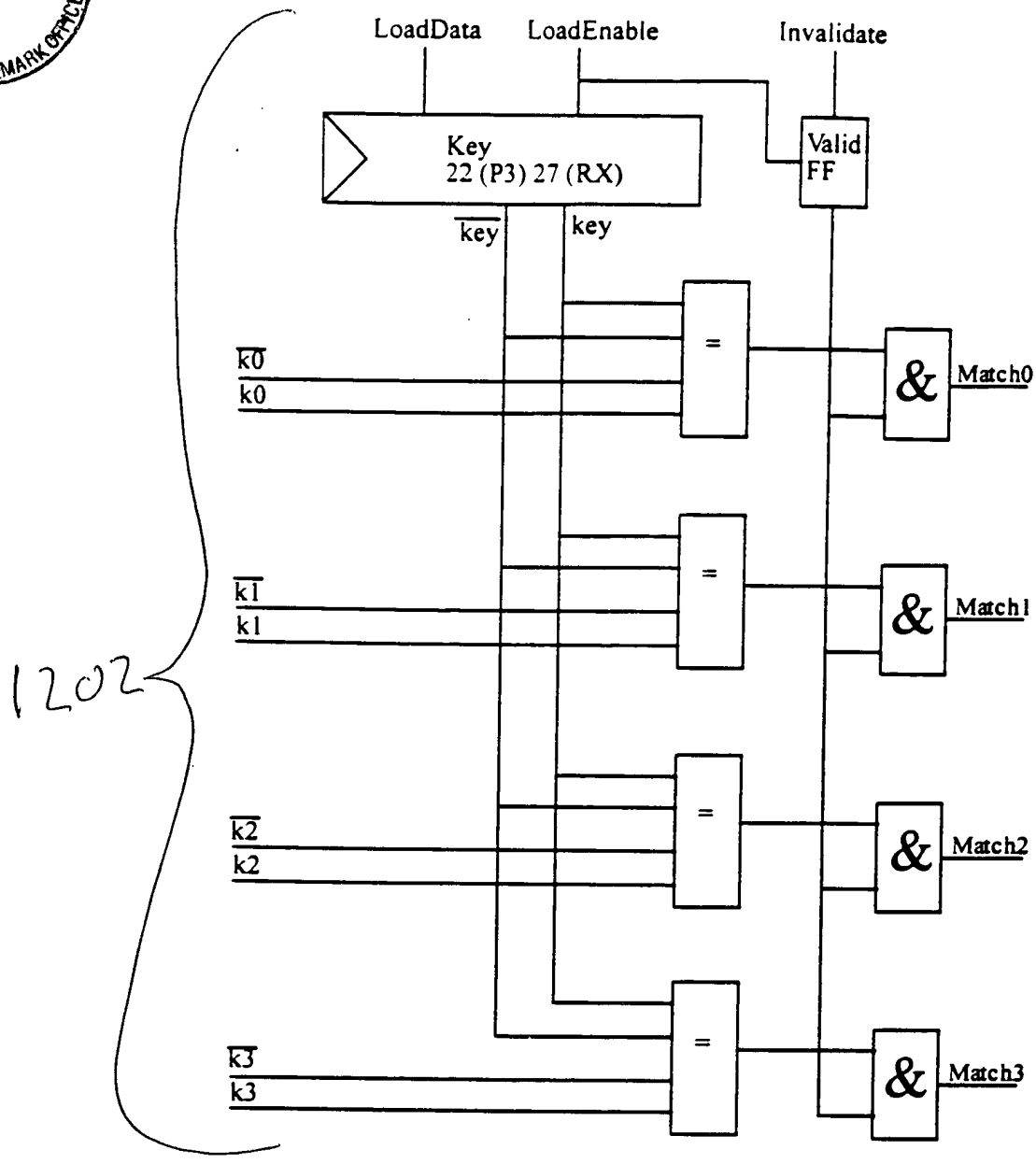


FIG. 13

TLB 1040

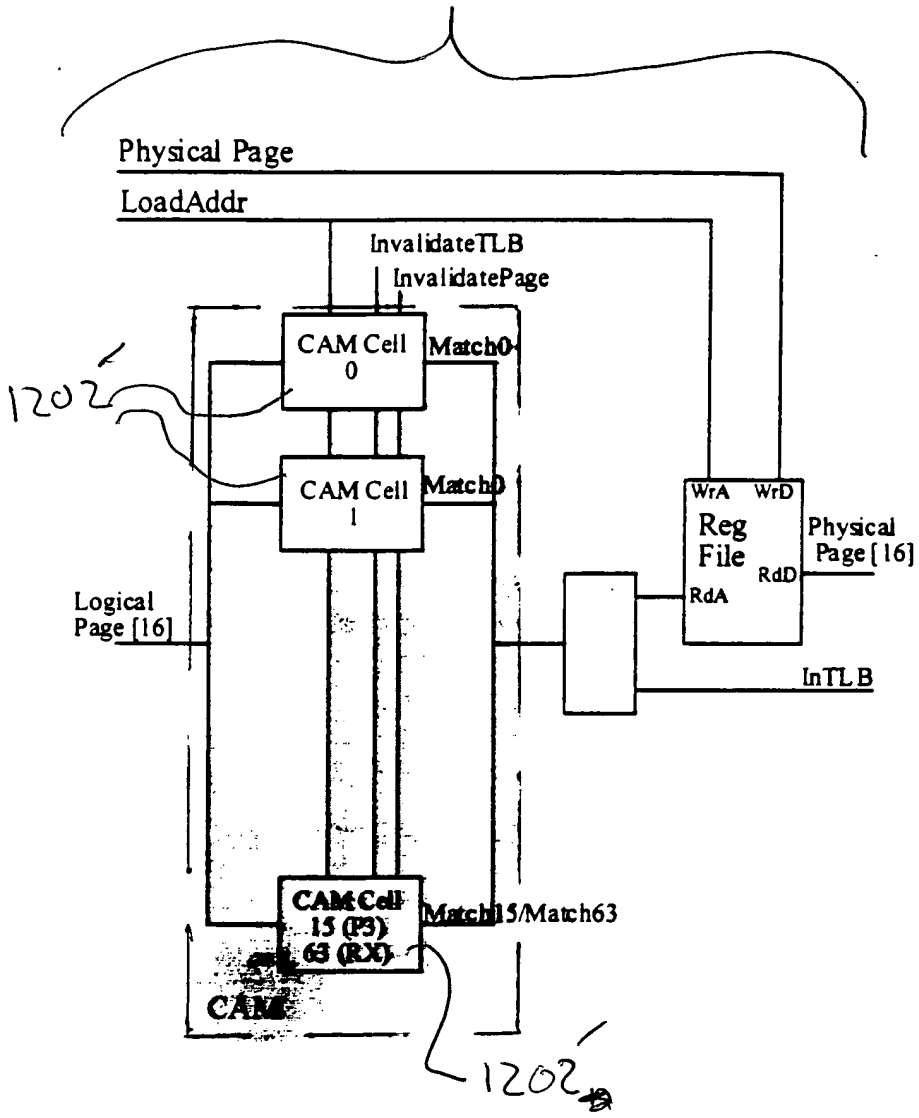


FIG. 14

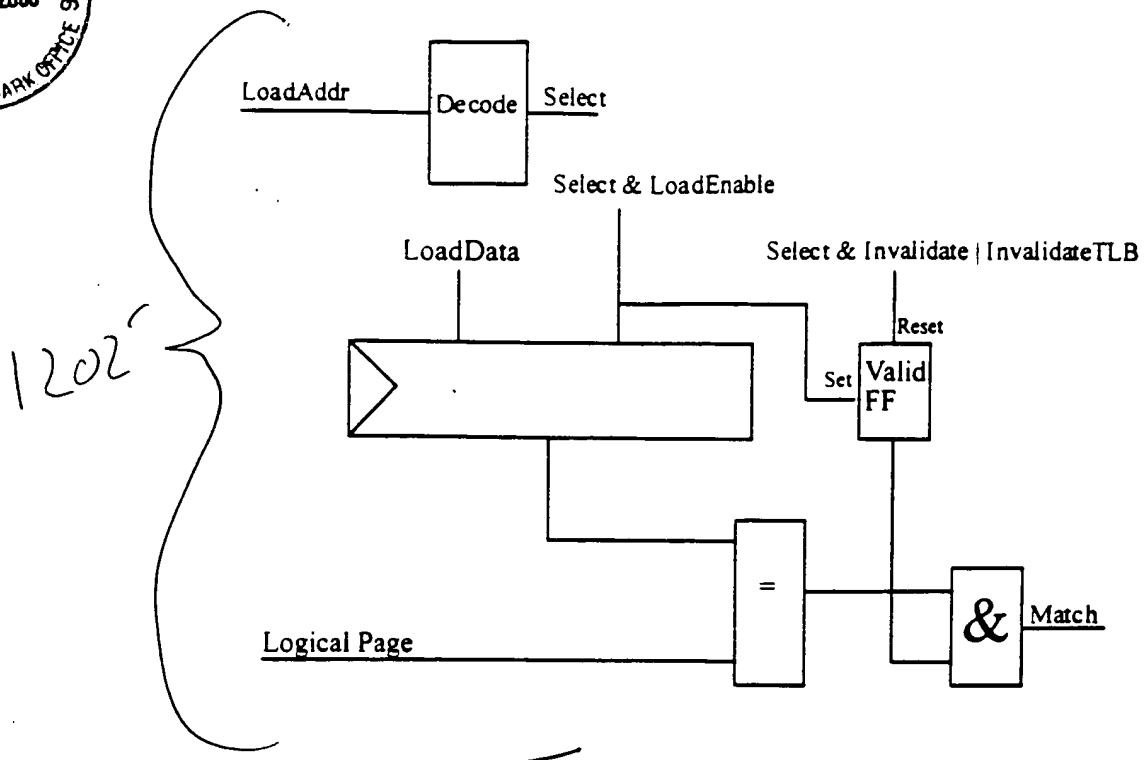


FIG. 15

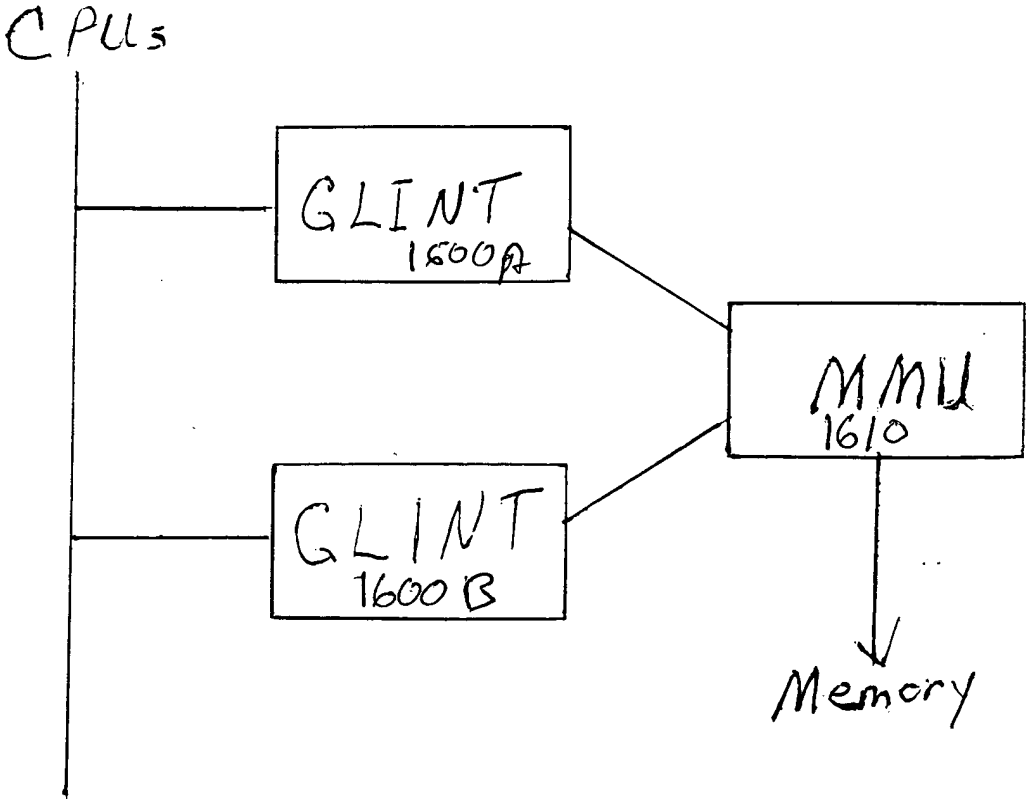


FIG. 16